E.G.S.PILLAYENGINEERINGCOLLEGE

(Autonomous)

Approved byAICTE,NewDelhi|Affiliated to AnnaUniversity, Chennai Accredited byNAAC with „A"Grade|AccreditedbyNBA(CSE, EEE, MECH)

NAGAPATTINAM–611002

B.E.Electronicsand CommunicationEngineering

FullTimeCurriculumand Syllabus

FourthYear– EighthSemester

Course Code	CourseName	L	T	P	C	Maximum Marks		
						CA	ES	Total
Theory Course								
	Professional Elective -VII	3	-	-	3	40	60	100
	Professional Elective -VIII	3	-	-	3	40	60	100
	Professional Elective - IX	3	-	-	3	40	60	100
LaboratoryCourse								
1704EC851	Project Work	-	-	18	9	50	50	100
	Total	**9**	**-**	**18**	**18**	**170**	**230**	**400**
Professional Elective - VII								
1703EC027	Multimedia Communication	3	0	0	3	40	60	100
1703EC028	Wireless Sensor Networks	3	0	0	3	40	60	100
1703EC029	Radar and Navigation Aids	3	0	0	3	40	60	100
1703EC030	Microwave Integrated Circuits	3	0	0	3	40	60	100
1703EC031	Satellite Communication	3	0	0	3	40	60	100
Professional Elective – VIII								
1703EC032	System-on Chip Design	3	0	0	3	40	60	100
1703EC033	Network on Chip Design	3	0	0	3	40	60	100
1703EC034	Low Power VLSI Design	3	0	0	3	40	60	100
1703EC035	Analog IC Design	3	0	0	3	40	60	100
1703EC036	Mixed Signal CMOS Design	3	0	0	3	40	60	100

Professional Elective - IX								
1703EC037	Electromagnetic Interference and Compatibility	3	0	0	3	40	60	100
1703EC038	Digital System Design and Testing	3	0	0	3	40	60	100
1703EC039	Optical Networks	3	0	0	3	40	60	100
1703EC040	RF MEMS	3	0	0	3	40	60	100
1703EC041	Digital Switching and Transmission	3	0	0	3	40	60	100
1703EC042	ARM Processors	3	0	0	3	40	60	100
1703EC043	Mobile Computing	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE – VII

1703EC027	MULTIMEDIA COMMUNICATIONS	L	T	P	C
		3	0	0	3

UNIT I IntroductiontoMultimedia Communications 5 Hours

Componentsofmultimediasystem,Desirable features,Applicationsofmultimediasystems, Introductiontodifferent types,Multimedia storage device.

UNIT II Digital audio representation 9 Hours

Digital audio representationandprocessing-timedomainand transformdomain representations.Codingstandards, transmissionandprocessingofdigitalaudio.Musical instrument synthesizers.

UNIT III Imagecodingalgorithms 12 Hours

Stillimagecoding-JPEG.DiscretecosineTransform.SequentialandProgressiveDCT based encodingalgorithms,lossless coding,hierarchicalcoding.Basicconceptsofdiscrete wavelettransformcodingandembeddedimagecodingalgorithms. Introductionto JPEG2000.

UNIT IV MPEG 9 Hours

Feature ofMPEG1,structureofencodinganddecodingprocess,MPEG2enhancements, and differentblocksofMPEGvideo encoder.

UNIT V Videocoding 10 Hours

Contentbasedvideocoding-overview ofMPEG4video,motionestimationand compensation. Different codingtechniquesandverificationmodels. Block diagramofMPEG4videoencoderanddecoder.AnoverviewofH261 andH263video coding techniques

TOTAL: 45

REFERENCES:

1. Fred Halsall, "**Multimedia Communications**", Pearson education, 2001
2. J.S. Chitode, **"Information coding techniques"**, Technical publications, 1st edition 2007.
3. Raifsteinmetz, Klara Nahrstedt, "**Multimedia: Computing, Communications and Applications**", Pearson education, 2002
4. John Billamil, Louis Molina, "**Multimedia : An Introduction**", PHI, 2002

1702EC603	WIRELESS NETWORKS AND STANDARDS	L	T	P	C
		3	0	0	3

UNIT I Overview of Wireless Sensor Networks and Wireless Transmission 9 Hours

Introduction of WSN, Basic Overview of the Technology, Range of Applications, Examples of WSN Applications, Frequencies for radio transmission, Signals, Antenna, Signal Propagation, Multiplexing, Modulation, Spread Spectrum.

UNIT II Multiple Access Techniques 9 Hours

Introduction, Narrowband Channelized Systems, Spectral Efficiency, Wideband Systems, Comparisons of FDMA, TDMA, and DS-CDMA, Capacity of DS-CDMA System, Comparison of DS-CDMA vs. TDMA System Capacity, Frequency Hopping Spread Spectrum with M-ary frequency Shift Keying, Orthogonal Frequency Division Multiplexing (OFDM), Multicarrier DS-CDMA (MC-DS-CDMA), Random Access Methods, Idle Signal Casting Multiple Access, Packet Reservation Multiple Access, Error Control Schemes for Link Layer.

UNIT III Routing and Transport Control Protocols for Wireless Sensor Networks 9 Hours

Introduction, Data Dissemination and Gathering, Routing Challenges and Design Issues in Wireless
Sensor Networks, Routing Strategies in Wireless Sensor Networks, Traditional Transport Control Protocols, Transport Protocol Design Issues, Examples of Existing Transport Control Protocols, Performance of Transport Control Protocols

UNIT IV Localization and positioning 9 Hours

Properties of localization and positioning procedures, Possible approaches, Mathematical basics for the lateration problem, Single-hop localization, Positioning in multihop environments, Topology control - Motivation and basic ideas, Controlling topology in flat networks, Hierarchical networks by dominating sets, Hierarchical networks by clustering, Combining hierarchical topologies and power control, Adaptive node activity

UNIT V Security in Wireless Systems and Wireless Application Protocol 9 Hours

Security and Privacy Needs of a Wireless System, Required Features for a Secured Wireless Communications System, Methods of Providing Privacy and Security in Wireless Systems, Wireless Security and Standards, IEEE 802.11 Security, Security in North American Cellular/PCS Systems, Security in GSM, GPRS, and UMTS, Data Security, Air Interface Support for Authentication Methods, WAP Programming Model, WAP Architecture, WAP Advantages and Disadvantages, Applications of WAP, imode versus WAP

TOTAL: 45 Hours

REFERENCES:

1. Jochen Schiller, ”Mobile Communications”, Second Edition, Pearson Education 2012.
2. Vijay Garg, “Wireless Communications and networking”, First Edition, Elsevier 2007.
3. Kazem Sohraby, “Wireless Sensor Networks Technology, Protocols and Applications”, Wiley Interscience 2007.
4. Holger Karl, **“**Protocols and architectures for Wireless Sensor Networks”, John Wiley & Sons 2005.

\

1703EC028	WIRELESS SENSOR NETWORKS	L	T	P	C
		3	0	0	3

UNIT I WIRELESS NETWORK ARCHITECTURE 9 Hours

Introduction-Wireless network logical architecture – Network physical architecture- Wireless LAN standards: System architecture, protocol architecture, physical layer, MAC layer, 802.11 Enhancements – Hiper LAN: WATM, BRAN, HiperLAN2 – Bluetooth- VoWLAN and VoIP security – WPA- IEEE802.16-WIMAX: Physical layer, MAC, Spectrum allocation for WIMAX

UNIT II ADHOC AND SENSOR NETWORKS 9 Hours

Introduction - Mobile IP: IP packet delivery, Agent discovery, tunneling and encapsulation, IPV6- Mobile ad-hoc network: Routing, Destination Sequence distance vector, Dynamic source routing- Characteristics of MANETs, Table-driven and Source-Initiated On Demand routing protocols, Hybrid protocols, Wireless Sensor networks-Classification, MAC and Routing protocols.

UNIT III PROTOCOLS AND TCP/IP SUITE 9 Hours

The Need for a Protocol Architecture - The TCP/IP Protocol Architecture - The OSI Model - Internetworking TCP enhancements for wireless protocols - Traditional TCP: Windows based Congestion control, fast retransmit/fast recovery, Influences of mobility on TCP mechanism - Classical TCP improvements: Indirect TCP, Snooping TCP, Mobile TCP, Time out freezing, Selective retransmission, Transaction oriented TCP - TCP over 3G wireless networks

UNIT IV DESIGN OF WIRELESS WIDE AREA NETWORK 9 Hours

Basics of indoor RF planning- Three phases of wireless network design- Overview of UTMS Terrestrial Radio access network-UMTS Core network Architecture: link budgets for GSM, CDMA, 3G-MSC, 3G- SGSN, 3G-GGSN, SMS-GMSC/SMS-IWMSC, Firewall, DNS/DHCP-High speed Downlink packet access (HSDPA)systems - LTE network architecture and protocol.

UNIT V CURRENT AND FUTURE OF WIRELESS NETWORKING TECHNOLOGY 9 Hours

Introduction – 4G vision – 4G features and challenges - Applications of 4G – Leading edge WNT: Wireless mesh network routing- Network independent roaming- Gigabit wireless LANs- OFDM-MIMO systems, Adaptive Modulation and coding with time slot scheduler, Cognitive Radio.

TOTAL: 45 Hours

REFERENCES:

1. Erik Dahlman, Stefan Parkvall, Johan Skold and Per Beming, "3G Evolution HSPA and LTE for Mobile Broadband", Second Edition, Academic Press, 2008.
2. Anurag Kumar, D.Manjunath, Joy kuri, "Wireless Networking", First Edition, Elsevier 2011.
3. Simon Haykin , Michael Moher, David Koilpillai, "Modern Wireless Communications", First Edition, Pearson Education 2013

1703EC029 RADAR AND NAVIGATION AIDS

L	T	P	C
3	0	0	3

UNIT I RADAR EQUATIONS **9 Hours**

RADAR Block Diagram & operation- RADAR Frequencies- RADAR Equation- Detection of signals in Noise- RADAR cross section of targets- RADAR cross section fluctuations- transmitter power- pulse repetition frequency- system losses and propagation effects

UNIT II MTI AND PULSE DOPPLER RADAR **9 Hours**

Introduction to Doppler & MTI RADAR- Delay Line canceller- Moving Target Detector- Pulse Doppler RADAR- Non-Coherent MTE- CW RADAR- FMCW RADAR- Tracking RADAR- Monopulse Tracking – Conical Scan and Sequential Lobing.

UNIT III RADAR SIGNAL DETECTION AND PROPAGATION ON WAVES **9 Hours**

Detection criteria- automatic detection- constant false alarm rate receiver- information available from a RADAR- ambiguity diagram- pulse compression- introduction to clutter- surface clutter RADAR equation- anomalous propagation and diffraction.

UNIT IV TRACKING ,IMAGING AND SCANNING RADAR **9 Hours**

Tracking with radar ,monopulse tracking ,conical scan and sequential lobing,low angle tracking ,air surveillance radar,Introduction to synthetic aperture radar ,tracking in range and Doppler ,acquisition Principle of phased array for electronic scanning ,and its operation .Radio ranges: LF/MF four course radio ranges ,VHF omni directional range ,vor receiving equipment, Hyperbolic system of navigation :LORAN,DECCA

UNIT V SATELLITE NAVIGATIONAL SYSTEM **9 Hours**

Instrument landing system, Ground controlled approach system,Microwave landing system,Distance measuring equipment ,TACAN Doppler navigation _Doppler effect,Track stabilization .SATELLITE navigation :GPS principle of operation ,position location determination,principle of GPS receiver and applications

TOTAL: 45 Hours

REFERENCES:

1. "Introduction to radar system", Merrill I.skolnik ,3rd edition Tata McGraw hill 2003 .
2. "Elements electronic navigation system",N.S.Nagaraja ,2nd edition Tata McGraw Hill 2000.
3. " Principle of Radar",J C Toomay ,PHI 2nd edition 2004.
4. " Radar Principles ',Peyton Z Peebles ,John Wiley ,2004.

1703EC030	MICROWAVE INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

UNIT I INTRODUCTION TO MICROWAVE CIRCUITS 9 Hours

Definitions – Frequency Bands – Lumped versus Distributed Circuits - Behavior of finite lengthtransmission lines – General Characteristics of PC Boards – Transmission Lines on PC Boards –Passives made from Transmission Lines – Resonators - Combiners, Splitters and Couplers

UNIT II MATCHING NETWORKS AND FILTER DESIGN 9 Hours

Circuit Representation of two port RF/Microwave Networks: Low Frequency Parameters, HighFrequency Parameters, Transmission Matrix, ZY Smith Chart, Design of Matching Circuits usingLumped Elements, Matching Network Design using Distributed Elements, Filter design.

UNIT III AMPLIFIERS AND OSCILLATORS 9 Hours

Amplifiers: Stability considerations in active networks – Gain Consideration in Amplifiers – NoiseConsideration in active networks – Broadband Amplifier design – Low Noise Amplifier Design,Oscillators: Oscillator versus Amplifier Design – Oscillation conditions – Design and stabilityconsiderations of Microwave Transistor Oscillators

UNIT IV MIXERS AND CONTROL CIRCUITS 9 Hours

Mixer Types – Conversion Loss – SSB and DSB Mixers – Design of Mixers: Single Ended Mixers –Single Balanced Mixers - Sub Harmonic Diode Mixers , Microwave Diodes , Phase Shifters – PINDiode Attenuators

UNIT V MICROWAVE IC DESIGN AND MEASUREMENT TECHNIQUES 12 Hours

Microwave Integrated Circuits – MIC Materials- Hybrid versus Monolithic MICs – Multichip ModuleTechnology - Fabrication Techniques, Miniaturization techniques, Introduction to SOC, SOP, Testfixture measurements, probe station measurements, thermal and cryogenic measurements,experimental field probing techniques.

TOTAL: 45 + 15 Hours

REFERENCES:

1. Thomas H.Lee, “Planar Microwave Engineering”, Cambridge University Press, 2004,
2. Matthew M. Radmanesh, “Radio Frequency and Microwave Electronics”, Pearson Education, II Edition 2002
3. “Microwave Transistor Amplifiers – Analysis and Design”, II Edition, Prentice Hall, New Jersy
4. Ravender Goyal, “Monolithic MIC; Technology & Design”, Artech House, 1989.
5. Gupta K.C. and Amarjit Singh, “ Microwave Integrated Circuits”, John Wiley, New York, 1975.
6. Hoffman R.K. “Handbook of Microwave Integrated Circuits”, Artech House, Boston, 198
7. Ulrich L. Rohde and David P.N., “ RF / Microwave Circuit Design for Wireless Applications”, John Wiley, 2000.

1703EC031	SATELLITE COMMUNICATION	L	T	P	C
		3	0	0	3

UNIT I SATELLITE ORBITS **9 Hours**

Introduction - Spectrum allocations for satellite systems -Kepler‘s Laws - orbital parameters - orbital perturbations - station keeping – Type of orbits - Geo stationary orbits – look angle determination- limits of visibility – eclipse -sub satellite point – sun transit outage - launching procedures - launch vehicles and propulsion.

UNIT II SPACE AND EARTH SEGMENT **9 Hours**

Spacecraft technology- structure- power supply- attitude and orbit control - thermal control and propulsion - communication subsystems - telemetry, tracking and command - TranspondersAntenna subsystem, Equipment reliability. Earth station technology -Receive only home TV systems - MATV – CATV – Transmit Receive Earth Stations.

UNIT III SATELLITE ACCESS **9 Hours**

Modulation and Multiplexing-Voice, Data, Video, Analog – digital transmission system-Digital video broadcast - multiple access: FDMA, TDMA, CDMA- assignment methods -spread spectrum communication -compression – encryption. Mobile satellite Service: GSM, GPS,communication between satellites

UNIT IV SATELLITE LINK DESIGN **9 Hours**

Introduction- Equivalent isotropic radiated power -Transmission Losses – Link power budget equation - System Noise, Carrier to Noise ratio – uplink – downlink – effects of rain – combined uplink and downlink C/N ratio – inter modulation noise - Interference between satellite circuits.

UNIT V SATELLITE APPLICATIONS **12 Hours**

Satellite mobile services – VSAT- Radarsat- GPS- Orbcomm-iridium- Direct Broadcast satellites (DBS) - Direct to home Broadcast (DTH) -Digital audio broadcast (DAB) – World space services, Business TV (BTV) – GRAMSAT - Specialized services: E mail, Video conferencing, Internet- INTELSAT Series- INSAT – INMARSAT. Remote sensing

TOTAL: 45 Hours

REFERENCES:

1. Wilbur L.Pritchard, Hendri G. Suyderhoud, Robert A. Nelson, “Satellite Communication SystemsEngineering”, Prentice Hall/Pearson, 2007.
2. N.Agarwal, “Design of Geosynchronous Space Craft”, Prentice Hall, 1986.
3. Bruce R. Elbert, “The Satellite Communication Applications”, Hand Book, Artech House BostanLondon, 1997.
4. Tri T. Ha, “Digital Satellite Communication”, II nd edition, 1990.
5. Emanuel Fthenakis, “Manual of Satellite Communications”, Mc Graw Hill Book Co., 1984.
6. Robert G. Winch, “Telecommunication Trans Mission Systems”, Mc Graw-Hill Book Co., 1983
7. Brian Ackroyd, “World Satellite Communication and earth station Design”, BSP professionalBooks, 1990.
8. G.B.Bleazard, “Introducing Satellite communications“, NCC Publication, 1985.
9. M.Richharia, “Satellite Communication Systems-Design Principles”, Macmillan 2003.

PROFESSIONAL ELECTIVES – VIII

1703EC032	SYSTEM ON CHIP DESIGN	L	T	P	C
		3	0	0	3

UNIT I : SYSTEM ARCHITECTURE: OVERVIEW **9 Hours**

Components of the system –Processor architectures –Memory and addressing –system level interconnection –SoC design requirements and specifications –design integration –design complexity –cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC **9 Hours**

Overview –soft processors, processor core selection. Basic concepts–instruction set, branches, interrupts and exceptions. Basic elements in instruction handling –Minimizing pipeline delays –reducing the cost of branches –Robust processors –Vector processors, VLIW processors, Superscalar processors.

UNIT III MEMORY DESIGN **9 Hours**

SoC external memory, SoC internal memory, Scratch pads and cache memory –cache organization and write policies –strategies for line replacement at miss time –split I-and D-caches –multilevel caches –SoC memory systems –board based memory systems –simple processor/memory interaction

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION **9 Hours**

Bus architectures –SoC standard buses –AMBA, CoreConnect –Processor customization approaches Reconfigurable technologies –mapping designs onto reconfigurable devices -FPGA based design –Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V FPGA BASED EMBEDDED PROCESSOR **9 Hours**

Hardware software task partitioning –FPGA fabric Immersed Processors –Soft Processors and Hard Processors –Tool flow for Hardware/Software Co-design–Interfacing Processor with memory and peripherals –Types of On-chip interfaces –Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller -FPGA-based Signal Interfacing and Conditioning

TOTAL: 45 Hours

REFERENCES:

1. Michael J. Flynn and Wayne Luk, Computer System Design: System-on-Chip", John Wiley and sons, 2011
2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable GateArrays", Springer Verlag London Ltd., 2009.
3. Sudeep Pasricha and NikilDutt,On-Chip Communication Architectures-System on Chip Interconnect, Elsevier, 2008
4. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
5. Wayne Wolf Modern VLSI Design – IP based Design", Prentice Hall, 4th Edition, 2008.

1703EC033	NETWORK ON CHIP	L	T	P	C
		3	0	0	3

UNIT I ICN ARCHITECHTURE **9 Hours**

Introduction - Classification of ICNs - Topologies - Direct networks - Indirect networks-Performance analysis

UNIT II SWITCHING TECHNLOGIES **9 Hours**

Basic switching techniques - Virtual channels - Hybrid switching techniques Optimizing switching techniques - Comparison of switching techniques - Deadlock, livelock and Starvation

UNIT III ROUTING TECHNOLOGIES **9 Hours**

Taxonomy of routing algorithms - Deterministic routing algorithms - Partially adaptive algorithms - Fully adaptive algorithms - Routing in MINs - Routing in switch-based networks with irregular topologies - Resource allocation policies- Flow control.

UNIT IV NETWORK ON CHIP **9 Hours**

NoC Architectures - Router architecture - Area, energy and reliability constraints - NoC design lternatives- uality-of Service (QoS) issues in NoC architectures

UNIT V EMERGING TRENDS **9 Hours**

. Fault-tolerance issues - Emerging on-chip interconnection technologies- 3D NoC- Simulation

TOTAL: 45 Hours

REFERENCES:

1. Jose Duato, Sudhakar Yalamanchili, Lionel Ni, "Interconnection Networks: An EngineeringApproach", Morgan Kaufmann, 2002
2. William James Dally, Brian Towles, "Principles and Practices of Interconnection Networks", Morgan Kaufmann, 2004
3. Giovanni De Micheli, Luca Benini, "Networks on Chips: Technology and Tools", Morgan Kaufmann, 2006
4. Natalie D. Enright Jerger, Li-ShiuanPeh, “On-Chip Networks (Synthesis Lectures on Computer Architecture)”, Morgan and Claypool, 2004
5. Fayez Gebali, Haytham Elmiligi, Mohamed Wathed El-Kharashi, “Networks-on-Chips: Theory and Practice”, CRC Press, 2009

1703EC034	LOW POWER VLSI DESIGN	L	T	P	C
		3	0	0	3

UNIT I POWER DISSIPATION IN CMOS **9 Hours**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9 Hours**

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9 Hours**

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION **9 Hours**

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9 Hours**

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 Hours

REFERENCES:

1. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
2. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
3. DimitriosSoudris, ChirstianPignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
4. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
5. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
6. AbdelatifBelaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.

1703EC035	ANALOG IC DESIGN	L	T	P	C
		3	0	0	3

UNIT I MOS DEVICES AND CIRCUITS **9 Hours**

Evolution of ICs - VLSI design flow - Device modeling -Moore_s law- MOS transistors- depletion and enhancement mode operations - NMOS and CMOS inverter circuits - Stick diagram and Layout diagram- Two input NAND and NOR circuits using CMOS

UNIT II FABRICATION OF ICS **9 Hours**

NMOS and CMOS fabrication - N-well, P-well and twin tub processes

UNIT III IMPLEMENTATION STRATEGIES **9 Hours**

PLDs – PAL, PLA, CPLD, Full custom and Semi custom ASIC design- Standard cell design, FPGA building block architectures, FPGA interconnect - Routing – FPGA, Xilinx 4000 series - Altera Cyclone III

UNIT IV CURRENT TRENDS **9 Hours**

BiCMOS and GaAs devices- Introduction to Low power VLSI circuit techniques - Introduction to analog and mixed signal design.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE **9 Hours**

Introduction to Verilog HDL –Behavior modeling -Tasks and functions -Verilog structure, syntax and semantics, Gate level modeling - Dataflow modeling Design examples - Adders, Multiplexers, Flip Flops, Registers , counters

TOTAL: 45 Hours

REFERENCES:

1. Pucknell D.A and EshraghianK ,"Basic VLSI Design‖, PHI publication, Second Edition, 2011.
2. Charles H. Roth , ―Digital Systems Design Using VHDL‖, CL Engineering/Cengage Learning India, 2012.
3. Samir Palnitkar, ―Verilog HDL Guide to Digital design and synthesis‖, Second Edition Pearson Education, 2009.
4. M.J. Smith, ‖Application specific integrated circuits‖, Addison Wesley, 2008.
5. West N and EshraghianK,―Principles of CMOS VLSI Design‖, Addison Wesley Publication, Second Edition, 1993.

1703EC036	MIXED SIGNAL CMOS DESIGN	L	T	P	C
		3	0	0	3

UNIT I CMOS AMPLIFIERS BASICS **9 Hours**

Introduction to MOS Capacitances- passive components and their parasitic- small and large signal odelling and analysis- Different Single stage and Differential Amplifiers- Current Mirrors.

UNIT II MULTI-STAGE AMPLIFIERS **9 Hours**

Telescopic and Folded cascode amplifiers- Slew-rate, Pole splitting-Two-stage amplifiers – analysis- Frequency response- Stability compensation- Common mode feedback analysis-feedback amplifier topologies.

UNIT III CIRCUIT DESIGN **9 Hours**

Custom Circuit design-Cell based and Array based design implementations- Static and Dynamic Characteristics of CMOs inverter-Power dissipation-Logical effort- Module 2 Designing combinational and sequential circuits.

UNIT IV LOGIC CIRCUITS **9 Hours**

Static CMOS design- Different styles of logic circuits-Logical effort of complex gates-Static and dynamic properties of complex gates- Dynamic CMOS Logic- Timing metrics of sequential circuits- Dynamic latches and Registers-Pipelining.

UNIT V CIRCUIT CHARACTERIZATION **9 Hours**

Circuit characterization and performance estimation – Resistance-Capacitance estimation - Switching characteristics - Delay models –Timing issues in Digital circuits-Power dissipation-Impact of Clock Skew and Jitter.

TOTAL: 45 Hours

REFERENCES:

1. R.Jacob Baker, ”CMOS Mixed-Signal Circuit Design”, John Wiley & Sons, 2008.
2. VineethaP.Gejji Analog and Mixed Mode Design - Prentice Hall, 1st Edition , 2011
3. “Analog Integrated Circuit Design” by Tony Chan Carusone, David A. Johns, Kenneth W. Martin Reference books:2011,.
4. “Analog Design Essentials” by Willy M. C. Sansen,2010
5. “Design of Analog CMOS Integrated Circuits” by Behzad Razavi,2002.

1703EC037	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

UNIT I PRINCIPLES OF EMI AND EMC **9 Hours**

Definition of EMI and EMC with examples – Classification of EMI/EMC – CE, RE, CS, RS – Units of Parameters –Sources of EMI – EMI coupling modes – CM and DM – ESD Phenomena and effects – Transient phenomena andsuppression.

UNIT II EMI MEASUREMENTS **9 Hours**

Basic principles of RE, CE, RS and CS measurements – EMI measuring instruments – Antennas – LISN – Feed through capacitor – Current probe – EMC analyzer and detection technique open area site – Shielded anechoicchamber – TEM cell.

UNIT III EMC STANDARD AND REGULATIONS **9 Hours**

National and International standardizing organizations – FCC, CISPR, ANSI, DOD, IEC, CENEEC, FCC CE and REstandards – CISPR, CE and RE Standards, IEC/EN, CS standards – Frequency assignment – spectrumconversation.

UNIT IV EMI CONTROL METHODS AND FIXES **9 Hours**

Shielding – Theory and materials, Grounding, Bonding – General procedure and guidelines, Filtering – characteristics of filters – Power line filter – Filter evaluation and filter installation, EMI gasket, Isolation transformer,opto isolator.

UNIT V EMC DESIGN AND INTERCONNECTION TECHNIQUES **9 Hours**

Cable routing and connection – Component selection and mounting – PCB design – Trace routing – Impedance control – Decoupling – Zoning and grounding.

TOTAL: 45 Hours

REFERENCES:

1. Keiser, “Principles of Electromagnetic Compatibility” , 3rd Edition , Artech House, 1994.
2. C.R.Paul, “Introduction to Electromagnetic Compatibility”, John Wiley and Sons, 2006.
3. Prasad Kodali, V., “Engineering Electromagnetic Compatibility”, S. Chand and Co, 2000.
4. .Donwhite Consultant Incorporate – Handbook of EMI / EMC – Vol I – 1985.
5. Henry W. Ott, “Noise Reduction Techniques in Electronic Systems”, John Wiley & Sons, 2 Edition, 1988.

1703EC038	DIGITAL SYSTEM DESIGN AND TESTING	L	T	P	C
		3	0	0	3

UNIT I VERILOG HDL AND TEST BENCHES **9 Hours**

Importance of HDL, Design Methodologies, Basic Concepts - Lexical Conventions - Data Types - Verilog Operators - Modules and Ports - Gate Level, Dataflow, Behavioural - Verilog Test Benches

UNIT II ADVANCED VERILOG HDL AND SYSTEM DESIGN **9 Hours**

Switch Level Modeling - User Defined Primitives (UDP) - Timing and Delays - ALU - Barrel Shifter - Random Number Generator - Traffic Light Controller - Vending Machine Controller – Single Port RAM Design- FIFO -PCI Arbiter Design

UNIT III ASIC DESIGN **9 Hours**

ASIC Design Flow - Types of ASICs - ASIC Design EDA tools – Analysis - DC, Transient, AC andParametric Sweep Analysis - Design Synthesis - Floor Plan, Constructive & Iterative Partition andPlacement Algorithm - Lee Maze Routing Algorithm - Physical Verification

UNIT IV PROGRAMMABLE ASIC **9 Hours**

PROM, PLA, PAL ,CPLD Programmable IC Technologies - Introduction to FPGA – FPGAImplementation Process – FPGA EDA Tools - FPGA Internal Architectures - Actel ACT1 -Shannon's expansion theorem - Function generators - Xilinx XC3000 - Programmable Interconnections

UNIT V TESTING OF VLSI CIRCUITS **9 Hours**

General Concepts - Faults in Digital Circuits - Fault Detection using Path Sensitization and BooleanDifference - Fault Simulation -Design For Testability (DFT) - Adhoc Design - Boundary Scan Test – Built InSelf Test (BIST) - BILBO – LOCST- STUMPS - Signature Analyzer

TOTAL: 45 Hours

REFERENCES:

1. Ming-Bo Lin, Digital System Designs and Practices using Verilog HDL and FPGAs, Wiley,2012.
2. Samir Palnitkar, Verilog HDL, Pearson Education, 2nd Edition, 2004
3. M.J.S .Smith, Application Specific Integrated Circuits, Pearson Education Inc., 2006.
4. Bob Zeidman, Designing with FPGAs and CPLDs, Elsevier, CMP Books, 2002.
5. P.K.Lala, Digital Circuit Testing and Testability, Academic Press, 1997
6. M.Abramovici, M.A.Breuer and A.D.Friedman, Digital Systems and Testable Design, Jaico Publishing House, 2004.

1703EC039	OPTICAL NETWORKS	L	T	P	C
		3	0	0	3

UNIT I OPTICAL SYSTEM COMPONENTS 9 Hours

Light propagation in optical fibers – Loss & bandwidth, System limitations, Non-Linear effects; Solitons; Optical Network Components – Couplers, Isolators & Circulators, Multiplexers & Filters, Optical Amplifiers, Switches, Wavelength Converters.

UNIT II OPTICAL NETWORK ARCHITECTURES 9 Hours

Introduction to Optical Networks; SONET / SDH, Metropoliton-Area Networks, Layered Architecture ; Broadcast and Select Networks – Topologies for Broadcast Networks, Media-Access Control Protocols, Testbeds for Broadcast & Select WDM; Wavelength Routing Architecture.

UNIT III WAVELENGTH ROUTING NETWORKS 9 Hours

The optical layer, Node Designs, Optical layer cost tradeoff, Routing and wavelength assignment,Virtual topology design, Wavelength Routing Testbeds, Architectural variations.

UNIT IV PACKET SWITCHING AND ACCESS NETWORKS 9 Hours

Photonic Packet Switching – OTDM, Multiplexing and Demultiplexing, Synchronisation, Broadcast OTDM networks, Switch-based networks; Access Networks – Network Architecture overview, Future Access Networks, Optical Access Network Architectures; and OTDM networks.

UNIT V NETWORK DESIGN AND MANAGEMENT 9. Hours

Transmission System Engineering – System model, Power penalty - transmitter, receiver, Optical amplifiers, crosstalk, dispersion; Wavelength stabilization ; Overall design considerations; Control and Management – Network management functions, Configuration management, Performance management, Fault management, Optical safety, Service interface.

TOTAL: 45 Hours

REFERENCES:

1. Rajiv Ramaswami and Kumar N. Sivarajan, “Optical Networks : A Practical Perspective”, Harcourt Asia Pte Ltd., Second Edition 2004.

2. Siva Ram Moorthy and Mohan Gurusamy, “WDM Optical Networks :Concept,Design and Algorithms”, Prentice Hall of India, Ist Edition, 2002.

3. P.E. Green, Jr., “Fiber Optic Networks”, Prentice Hall, NJ, 1993.

1703EC040	RF MEMS	L	T	P	C
		3	0	0	3

UNIT I INTRODUCTION **9 Hours**

Overview of RF MEMS, Road map, fabrication process design and testing, Applications, RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation.

UNIT II MICRO MACHINED INDUCTORS AND CAPACITORS **9 Hours**

MEMS inductors and capacitors: Micro machined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.

UNIT III RF MEMS PHASE SHIFTERS **9 Hours**

MEMS phase shifters: Types. Limitations - Switched delay lines, Micro machined transmission lines, coplanar lines, Micro machined directional coupler and mixer.

UNIT IV MICRO MACHINED FILTERS ANTENNAS **9 Hours**

Micro machined RF filters: Modeling of mechanical filters, Electrostatic comb drive, Micromechanical filters using comb drives, Electrostatic coupled beam structures. Micro machined antennas: Micro strip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas.

UNIT V RF MEMS DESIGN ANALYSIS **9 Hours**

MEMS Physical Modeling, Physical and practical aspects of RF circuit design: X –Band RF MEMS Phase shifter for radar system applications, FBAR filter for PCS applications, A Ka-Band millimeterwave tunable filter. Impedance mismatch effects in RF MEMS, RF/Microwave substrate properties, MEMS-Resonators.

TOTAL: 45 Hours

REFERENCES:

1. V.K.Varadan, KJ.Vinoy,K.N.Jose, “RFMEMS and their Applications”, Wiley, 2003.
2. H.J.Delos Santos, “RF MEMS circuit Design for Wireless Communications”, Artech House, 2002.
3. Gabriel.M.Rebeiz, “RF MEMS Theory, Design and Technology”, John Wiley, 2003
4. Ulrich L, Rohde David P Razavi and NewKirk,” RF / Microwave Circuit Design”, John Wiley and Sons USA, 2000.
5. Rebeiz G.M,” RF MEMS: THEORY, Design and Technology”, John Wiley and Sons Inc., 2003
6. Matthew M Radmanesh, “Radio Frequency and Microelectronic Illustrated”, Pearson Education Asia Publication, 2002.

1703EC041	DIGITAL SWITCHING AND TRANSMISSION	L	T	P	C
		3	0	0	3

UNIT I EVOLUTION OF SWITCHING SYSTEMS 9 Hours

Introduction, Messageswitching, Circuitswitching, Functions of switching systems, Distribution systems, Electronicswitching, Digital switching systems, Basics of crossbar systems

UNIT II TELECOMMUNICATIONSTRAFFIC 9 Hours

Introduction, Unit of traffic, Congestion, Trafficmeasurement, Mathematical model, lostcallsystems, Queuing systems, Problems

UNIT III DIGITAL SWITCHING SYSTEMS 9 Hours

Fundamentals : Purposeof analysis, Basic central officelinkages, Outsideplant versus insideplant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, switching system fundamentals, Building blocks of adigital switching system, Basic callprocessing

UNIT IV TIME DIVISION SWITCHING 9 Hours

Introduction, space and time switching, Time switching networks, Synchronization

UNIT V MAINTENANCE OF DIGITAL SWITCHING SYSTEM 9 Hours

Softwaremaintenance, Impact of softwarepatcheson digital switching system maintainability, Embedded patcherconcept, Genericprogram upgrade, Effect of firmwaredeployment on digital switching system, Firmware-software coupling, Diagnostic resolution rate

TOTAL: 45 Hours

REFERENCES:

1. Telecommunication andSwitching, Traffic and Networks - J E Flood: Pearson Education, 2002.
2. Digital Switching Systems, Syed R. Ali, TMH Ed 2002.
3. Digital Telephony-John C Bellamy: Wiley India3rdEd, 2000
4. Digital switching systems, V.S Bagad, Anjali Bagad, Technical publications, 2014.
5. Digital Switching Systems, Syed Riffact Ali, Tata McGraw-Hill Inc, New York, 2002.
6. Tomasi Wayne, Electronic Communications System: Fundamentals Through Advanced, 5th Edition, Pearson PrenticeHall,2005. (TK5101.T655E 2004)
7. M.T. Hills , Telecommunication Switching Principles, London : Allen and Unwin, 1979.

1703EC042	ARM PROCESSOR	L	T	P	C
		3	0	0	3

UNIT I Introduction to ARM Architecture and Assembly language Programming 9 Hours

The Acorn RISC Machine-Architectural inheritance -The ARM programmer's model- ARM development tool-Data processing instructions- Data transfer instructions -Control flow instructions- Writing simple assembly language programs

UNIT II ARM Organization and System Development 9 Hours

3-stage pipeline ARM organization-5-stage pipeline ARM organization-ARM instruction execution-ARM implementation-The ARM floating-point architecture-The ARM memory interface-The Advanced Microcontroller Bus Architecture (AMBA)- The ARM reference peripheral specification-The ARMulator-The ARM debug architecture.

UNIT III The ARM Instruction Set 9 Hours

Introduction- Exceptions -Conditional execution -Branch and Branch with Link (B, BL)- Branch, Branch with Link and exchange (BX, BLX)- Software Interrupt (SWI)- Data processing instructions- Multiply instructions-Count leading zeros (CLZ - architecture v5T only)-Single word and unsigned byte data transfer instructions-Half-word and signed byte data transfer instructions-Multiple register transfer instructions-Swap memory and register instructions (SWP) -status register to general register transfer instructions-General register to status register transfer instructions -

UNIT IV ARM Processor Cores and Memory Hierarchy 9 Hours

ARM7TDMI-ARM8-ARM9TDMI-ARM10TDMI- Memory size and speed- On-chip memory -Caches -Cache design - an example -Memory management

UNIT V Embedded ARM Applications and Operating Systems 9 Hours

The VLSI Ruby II Advanced Communication Processor-The VLSI ISDN Subscriber Processor-The OneC™ VWS22100 GSM chip-The Ericsson-VLSI Bluetooth Baseband Controller-The ARM7500 and ARM7500FE -An introduction to operating systems-The ARM system control coprocessor- CP15 protection unit registers -ARM protection unit-CP15 MMU registers-ARM MMU architecture-Synchronization- Context switching

TOTAL: 45 Hours

REFERENCES:

1. "ARM System-on-Chip Architecture" by Steve Furber, Addison-Wesley Professional; 2 edition, August 14, 2000.
2. "Modeling and Simulation of ARM Processor Architecture: Using System C" by Mitesh Limachiaand Nikhil Kothari LAP LAMBERT Academic Publishing , June 29, 2012.
3. "Mobile Unleashed: The Origin and Evolution of ARM Processors in Our Devices" by Don Dingee and Daniel Nenni, CreateSpace Independent Publishing Platform; 1 edition, December 8, 2015.
4. "ARM Assembly Language: Fundamentals and Techniques" by William Hohl and Christopher Hinds, CRC Press; 2 edition, 10 December 2014.
5. "Introduction to Microprocessor Based Systems Using the ARM Processor" by Kris Schindler, Pearson Learning Solutions; 2 edition , January 8, 2013.
6. "ARM System Developer's Guide" by Andrew Sloss, Morgan Kaufmann, 10 May 2004.
7. "ARM processor" by Santul Bisht, LAP Lambert Academic Publishing, 25 November 2012.

1703EC043	MOBILE COMPUTING	L	T	P	C
	Professional(Open)Electives - IV	3	0	0	3

UNIT I INTRODUCTION **9 Hours**

Mobile Computing – Mobile Computing Vs wireless Networking – Mobile Computing Applications – Characteristics of Mobile computing – Structure of Mobile Computing Application. MAC Protocols –Wireless MAC Issues – Fixed Assignment Schemes – Random Assignment Schemes – ReservationBased Schemes.

UNIT II MOBILE INTERNET PROTOCOL AND TRANSPORT LAYER **9 Hours**

Overview of Mobile IP – Features of Mobile IP – Key Mechanism in Mobile IP – route Optimization.Overview of TCP/IP – Architecture of TCP/IP- Adaptation of TCP Window – Improvement in TCPPerformance.

UNIT III MOBILE TELECOMMUNICATION SYSTEM **9 Hours**

Global System for Mobile Communication (GSM) – General Packet Radio Service (GPRS) –Universal Mobile Telecommunication System (UMTS).

UNIT IV MOBILE AD-HOC NETWORKS **9 Hours**

Ad-Hoc Basic Concepts – Characteristics – Applications – Design Issues – Routing – Essential ofTraditional Routing Protocols –Popular Routing Protocols – Vehicular Ad Hoc networks (VANET) –MANET Vs VANET – Security.

UNIT V MOBILE PLATFORMS AND APPLICATIONS **9 Hours**

Mobile Device Operating Systems – Special Constrains & Requirements – Commercial MobileOperating Systems – Software Development Kit: iOS, Android, BlackBerry, Windows Phone – MCommerce– Structure – Pros & Cons – Mobile Payment System – Security Issues.

TOTAL: 45 Hours

REFERENCES:

1. Jochen H. Schller, “Mobile Communications”, Second Edition, Pearson Education, New Delhi,2007.
2. Prasant Kumar Pattnaik, Rajib Mall, “Fundamentals of Mobile Computing”, PHI Learning Pvt.Ltd, New Delhi – 2012.
3. Dharma Prakash Agarval, Qing and An Zeng, "Introduction to Wireless and Mobile systems",Thomson Asia Pvt Ltd, 2005.
4. Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, “Principles of Mobile Computing”, Springer, 2003.
5. William.C.Y.Lee,“Mobile Cellular Telecommunications-Analog and Digital Systems”, Second Edition,Tata Mc Graw Hill Edition ,2006.
6. C.K.Toh, “AdHoc Mobile Wireless Networks”, First Edition, Pearson Education, 2002.